Customer No. : 31561
Application No.: 10/707,677
Docket No. : 12089-US-PA

REMARKS

Present Status of Application

The Office Action dated March 14, 2005, rejected claims 1-4, 7-11 and 14-15 under 35 USC§102(e) as being anticipated by Yoo et al. (US Publication No. 2003/0211689A1). Claims 5-6 and 12-13 were rejected under 35 USC§103(a) as being unpatentable over Yoo et al. and in view of Reisinger et al. (US Patent No. 6,137,718).

Claims 7-8, 10-11 and 14-15 have been amended for correcting informalities and providing more descriptions, while claims 1-6 have been cancelled. No new matter has been added to the application by the amendments made to the specification, claims and drawings. This Amendment is promptly filed to place the above-captioned case in condition for allowance. After entering the amendments and considering the following discussions, a notice of allowance is respectfully solicited.

Discussion for 35 USC§102 and 103 rejections

Claims 1-4, 7-11 and 14-15 were rejected under 35 USC§102(e) as being anticipated by Yoo et al. (US Publication No. 2003/0211689A1). Claims 5-6 and 12-13 were rejected under 35 USC§103(a) as being unpatentable over Yoo et al. and in view of Reisinger et al. (US Patent No. 6,137,718).

The Applicant has carefully considered the remarks set forth in the Office Action.

Customer No. : 31561
Application No.: 10/707,677
Docket No. : 12089-US-PA

Claim 7 has been amended to provide more descriptions for clarification purposes, according to the present invention. Supporting grounds for this amendment can be found at least in figures 2A-2E and the related descriptions in the specification. Applicant respectfully asserts that claim 7 is patentably distinct from the prior art structures.

As amended, independent claim 7 recites:

7. A multi-level memory cell, comprising:
a substrate;
a gate disposed over the substrate;
a source region and a drain region configured in the substrate on each side of the gate;
a tunneling dielectric layer disposed between the gate and the substrate;
a charge-trapping layer disposed between the tunneling dielectric layer and the gate; and
*a top dielectric layer disposed between the charge-trapping layer and the gate, **wherein the top dielectric layer has at least two portions from the source region to the drain region, and the portions have different thicknesses, and wherein the tunneling dielectric layer has substantially a same thickness from the source region to the drain region.***

Yoo et al. merely discloses a non-volatile memory cell with non-planar gate insulating layers. The gate pattern 300 including (from top to bottom) the upper insulating pattern 165, the charge storage pattern 155 and the lower insulating pattern 112 and a tunnel insulating pattern 116 between the charge storage pattern 155 and the substrate 100. The tunnel insulating pattern 116 adjoining the drain region is thinner than the lower insulating pattern 112 adjoining the source region. That is, an insulating layer (112+116) under the charge storage pattern 155 is thinner on the drain region than on the

source region (paragraph [0064]).

The Office Action considered Yoo's pattern 165, 155 and 116 being respectively comparable to the top dielectric layer, charge-trapping layer and the tunneling dielectric layer of this application. Applicant respectfully disagrees with this consideration.

Yoo teaches a gate insulating layer consisting of a thicker lower insulating pattern 112 and a thinner tunnel insulating pattern 116 from the source to the drain. Obviously, Yoo fails to disclose the tunneling dielectric layer having substantially the same thickness from the source region to the drain region.

In Yoo's design, the thin tunneling insulating pattern 116 is designed to solve the problem of prior art's abnormal trapping regions (see page 1, paragraph [0014] of Yoo et al.). Since charges only penetrate the tunnel insulating pattern 116, the trapping region 400 is formed close to the drain region Moreover, Yoo employs "hot carrier injection" for programming.

Contrarily, in the design of the present invention, due to the top dielectric layer having at least two portions with different thicknesses and the tunneling dielectric layer of substantially the same thickness, charges will be trapped into the portion where the top dielectric layer has a thinner thickness first and then trapped into other portions which have thicker thickness sequentially. Therefore, a single memory cell can register multiple bits. According to the present invention, the tunneling of charges is performed through

Fowler-Nordheim tunneling effect.

Accordingly, the structure of the present invention is patentably distinct from the prior art reference Yoo. As a result, Yoo did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in independent claim 7. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Consequently, reconsideration and withdrawal of these 102 rejections are respectfully requested.

Regarding claims 5-6 and 12-13, the Office Action further relied on Reisinger et al. for teaching the thickness of the tunneling dielectric layer or the charge-trapping layer.

Claims 5-6 have been cancelled. As discussed above, the process of the present invention is patentably distinct from the prior art reference because Yoo fails to disclose all limitations of independent claim 7. Reisinger merely discloses a memory cell with a planar MOS transistor. However, even considering the teachings of Reisinger relating to the thickness, Reisinger fails to remedy the deficiencies of Yoo.

Therefore, it is respectfully submitted that claims 12-13 patentably distinguish over the cited references, either alone or in combination, for at least the reasons stated above as well as for the additional features that this claim recites.

Customer No. : 31561
Application No.: 10/707,677
Docket No. : 12089-US-PA

Withdrawal of these rejections under 35 USC 103(a) is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : June 14, 2005

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw;usa@jcipgroup.com.tw